What is claimed is:

1. A semiconductor memory device comprising:

a memory cell array portion including a memory cell portion and a source contact portion, said memory cell portion comprising:

a first memory cell transistor having a first gate electrode; and

a second memory cell transistor having a second gate electrode; and

a silicidation blocking layer on a source area on a substrate between said first gate electrode and said second gate electrode.

2. The semiconductor memory device as claimed in claim 1,

wherein said source areas has a step portion, and said silicidation blocking layer is formed on said step portion.

3. The semiconductor memory device as claimed in claim 2,

wherein said source contact portion comprises:

a source contact area; and

a silicide layer on said source contact area.

4. The semiconductor memory device as claimed in claim 1,

wherein said silicidation blocking layer covers side surfaces of said first

gate electrode.

5. The semiconductor memory device as claimed in claim 4,

wherein said silicidation blocking layer covers an upper surface of said first gate electrode.

6. The semiconductor memory device as claimed in claim 1,

wherein said silicidation blocking layer comprises a first side wall layer and a second side wall layer, said first side wall layer formed on a side surface of said first gate electrode, and said second side wall layer formed on a side surface of said first side wall and on a surface of said source area.

7. The semiconductor memory device as claimed in claim 6, further comprising:

a peripheral transistor portion having a peripheral transistor, said peripheral transistor having a peripheral transistor gate electrode;

wherein said second side wall layer is formed on a side surface of said peripheral transistor gate electrode.

8. The semiconductor memory device as claimed in claim 6,

wherein said source contact portion comprising:

~~a source contact area; and~~

a silicide layer on a surface of said source contact area.

9. A manufacturing method of a semiconductor memory device having a memory cell array portion comprising a memory cell portion and a source contact portion, comprising the steps of:

forming a first gate electrode, a first drain area and a first source area on said memory cell portion;

forming a second gate electrode, a second drain area and a second source area on said source contact portion;

forming a silicidation blocking layer on a surface of said first gate electrode, on a surface of said first drain area, on a surface of said first source area, on a surface of said second gate electrode, on a surface of said second drain area, and on a surface of said second source area; and

removing said silicidation blocking layer from an upper surface of said second gate electrode and said surface of said second source area without removing said silicidation blocking layer on said side surface of said second gate electrode and on said surface of said first source area.

10. The manufacturing method as claimed in claim 9, further comprising steps of:

forming a cover layer on said memory cell portion after said step of ~~forming said silicidation blocking layer ; and~~

etching said silicidation blocking layer by using said cover layer as a first mask.

11. The manufacturing method as claimed in claim 10, further comprising a step of:

forming a silicide layer on said surface of said second source area and said upper surface of said second gate electrode.

12. The manufacturing method as claimed in claim 9, further comprising steps of:

forming a cover layer on said surface of said first source area after said step of forming said silicidation blocking layer ; and

etching said silicidation blocking layer by using said cover layer as a second mask to remove said silicidation blocking layer from said first drain area and an upper surface of said first gate electrode.

13. The manufacturing method as claimed in claim 12, further comprising a step of:

forming a silicide layer on said upper surface of said first gate electrode, on said surface of said first drain area, on said upper surface of said second gate electrode, on said surface of said second source area and on said surface of said second drain area.

14. The manufacturing method as claimed in claim 9, further comprising a step of:

etching said silicidation blocking layer on said memory cell portion and on said source contact portion after said step of forming said silicidation blocking layer to remove said silicidation blocking layer on said upper surface of said first gate electrode and said surface of said first drain area without removing said silicidation blocking layer on said surface of said first source area.

15. The manufacturing method as claimed in claim 14, further comprising a step of:

forming a silicide layer on said upper surface of said first gate electrode, on said surface of said first drain area, on said upper surface of said second gate electrode and on said surface of said second source area.

16. The manufacturing method as claimed in claim 15,

wherein said silicidation blocking layer of said surface on said second source area is removed by said step of removing said silicidation blocking layer on said upper surface of said first gate electrode.

17. The manufacturing method as claimed in claim 9, further comprising steps of:

etching said silicidation blocking layer on said memory cell portion and on said source contact portion after said step of forming said silicidation blocking layer to remove said silicidation blocking layer from said upper surface of said first gate electrode and said surface of said first source area to remain at least a side surface of said first gate electrode;

forming a second silicidation blocking layer on said upper surface of said first gate electrode and on said surface of said first source area; and

etching said second silicidation blocking layer on said upper surface of said first gate electrode without removing said silicidation blocking layer on said surface of said first source area.

18. The manufacturing method as claimed in claim 17, further comprising a step of:

forming a silicide layer on said upper surface of said second gate electrode, on said surface of said second source area and on said upper surface of said first gate electrode.

19. The manufacturing method as claimed in claim 18,

wherein said second silicidation blocking layer is formed on a side surface of a gate electrode of a peripheral transistor on a peripheral transistor portion.

20. A manufacturing method of a semiconductor storage apparatus, comprising steps of:

forming an isolation oxide film on a silicon substrate;

forming a tunnel oxide film, a first layer of polysilicon and an interpoly insulating film on a memory cell portion;

forming a gate oxide film on a peripheral transistor portion;

forming a second layer of polysilicon on said memory cell portion and on said peripheral transistor portion;

covering said peripheral transistor portion with a mask;

etching said second layer of polysilicon, said interpoly insulating film, and said first layer of polysilicon to form a gate electrode of said memory cell portion;

covering said tunnel oxide film and said isolation oxide film on a first side of said gate electrode with a first mask;

removing said tunnel oxide film and said isolation oxide film on a second side of said gate electrode;

forming a source diffusion layer on said silicon substrate on said second side of said gate electrode;

forming a drain diffusion layer on said silicon substrate on said first side of said gate electrode;

forming a first insulating film on said memory cell portion and on said peripheral transistor portion;

covering said memory cell portion with a second mask;

etching said second layer of polysilicon to form a peripheral transistor gate electrode on said peripheral transistor portion;

forming a diffusion layer on said peripheral transistor portion; and

forming a silicide layer on a surface of said diffusion layers, on an upper surface of said peripheral transistor gate electrode.

21. The manufacturing method as claimed in claim 20, further comprising steps of:

etching said first insulating film to form a first side wall on a surfaee of said gate electrode on said memory cell portion; and

forming a silicide layer on an upper surface of said gate electrode and on a surface of said drain diffusion layer.

22. The manufacturing method as claimed in claim 21, further comprising a step of:

forming a second insulating film to form a second side wall on a surface of said first side wall, said second side wall filling a space next to said first side wall and above said source diffusion layer.

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